Electronic Version
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# REDUCED DIELECTRIC CONSTANT SPACER MATERIALS INTEGRATION FOR HIGH SPEED LOGIC GATES

## Abstract

An FET transistor has a gate disposed between a source and a drain; a gate dielectric layer disposed underneath the gate; and a spacer on a side of the gate. The gate dielectric layer is conventional oxide and the spacer has a reduced dielectric constant (k). The reduced dielectric constant (k) may be less than 3.85, or it may be less than 7.0 (~nitride), but greater than 3.85 (~oxide). Preferably, the spacer comprises a material which can be etched selectively to the gate dielectric layer. The spacer may be porous, and a thin layer is deposited on the porous spacer to prevent moisture absorption. The spacer may comprise a material selected from the group consisting of Black Diamond, Coral, TERA and Blok type materials. Pores may be formed in the spacer material by exposing the spacers to an oxygen plasma.